Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the above-identified application:

Listing of Claims:

1. (Currently Amended) A latch circuit having a total current and at least one output, the output having a first state and a second state, the output being controllable by a first trigger signal and a second trigger signal, the latch circuit comprising:

a SET circuit;

a RESET circuit; and

wherein at least one of the conditions from the group consisting of the following is true: 1) at the first state, the total current is conducted by the SET circuit, wherein the SET circuit switches when the first trigger signal is applied to the SET circuit, and wherein the first trigger signal ~~is less than 0.7 volts~~ creates a very small difference in voltage, and 2) at the second state, the total current is conducted by the RESET circuit, wherein the RESET circuit switches when the second trigger signal is applied to the RESET circuit, and wherein the second trigger signal ~~is less than 0.7 volts~~ creates a very small difference in voltage.

2. (Previously Presented) The latch circuit of claim 1, wherein the latch circuit forms a switching portion of a temperature-compensated oscillator circuit.

3. (Original) The latch circuit of claim 2, the temperature-compensated oscillator circuit further comprising level-shifting circuitry.

4. (Cancelled).

5. (Currently Amended) A method of oscillating the output of an oscillator, the output having a first state and a second state, the oscillator including a latch, the latch including a first latch transistor, a second latch transistor, a SET transistor and a RESET transistor, the method comprising:

at the first state, conducting a total current in the first latch transistor and the SET transistor such that the SET transistor is biased at a point close to a first threshold;

at the second state, conducting the total current in the second latch transistor and the RESET transistor such that the RESET transistor is biased at a point close to a second threshold;

varying the output from the first state to the second state by a first trigger signal to switch the SET transistor, wherein the first trigger signal ~~is less than the full Vbe voltage of the SET transistor~~ creates a very small difference in voltage; and

varying the output from the second state to the first state by a second trigger signal to switch the RESET transistor, wherein the second trigger signal ~~is less than the full Vbe voltage of the RESET transistor~~ creates a very small difference in voltage.

6. (Original) The method of claim 5 further comprising temperature compensating the oscillator.

7. (Previously Presented) An oscillator circuit comprising the latch circuit of claim 1, wherein the oscillator circuit further comprises an oscillator capacitor coupled to the SET circuit, such that, at the first state, the capacitor is substantially charged, and at the second state, the capacitor is substantially discharged.

8. (Previously Presented) The oscillator circuit of claim 7 further comprising a second current for charging the capacitor.

9. (Previously Presented) The oscillator circuit of claim 8, further comprising a current source for producing the second current.

10. (Previously Presented) The oscillator circuit of claim 9, further comprising an oscillator transistor coupled between the current source and the RESET circuit.

11. (Previously Presented) The oscillator circuit of claim 10, further comprising a source of electrical potential coupled to the base of the oscillator transistor.

12. (Previously Presented) The oscillator circuit of claim 10, further comprising temperature compensating circuitry for compensating the oscillator transistor, such that the difference between an upper oscillator threshold of the capacitor and a lower oscillator threshold of the capacitor remains constant.

13. (Previously Presented) The latch circuit of claim 1, wherein a de-bias circuit is coupled between the SET circuit and ground.

14. (Previously Presented) The latch circuit of claim 1, wherein a de-bias circuit is coupled between the RESET circuit and ground.

15. (Previously Presented) The latch circuit of claim 1, wherein the total current is provided by a plurality of current sources, and each of the plurality of current sources are coupled to a source of electrical potential.

16. (Previously Presented) The latch circuit of claim 1, wherein the total current is provided by two substantially equivalent current sources, and the current sources are coupled to a source of electrical potential.

17. (Previously Presented) The latch circuit of claim 1, wherein about one-half of the total current is provided by a first current source and about one-half of the total current is provided by a second current source, and the first and second current sources are coupled to a source of electrical potential.

18. (Previously Presented) The latch circuit of claim 1, wherein the total current is about 200 microamperes.

19. (Previously Presented) The latch circuit of claim 1, wherein, at the first state, the total current is substantially continuously conducted by the SET circuit.

20. (Previously Presented) The latch circuit of claim 1, wherein, at the second state, the total current is substantially continuously conducted by the RESET circuit.

21. (Previously Presented) The latch circuit of claim 1, wherein, when said first trigger signal is applied to said SET circuit, said RESET circuit switches ON.

22. (Previously Presented) The latch circuit of claim 1, wherein, when said second trigger signal is applied to said RESET circuit, said SET circuit switches ON.

23. (Previously Presented) The latch circuit of claim 1, wherein the first trigger signal is about 0.018 volts.

24. (Previously Presented) The latch circuit of claim 1, wherein the second trigger signal is about 0.018 volts.

25-37. (Cancelled).

38. (Previously Presented) The method of claim 5, wherein the first trigger signal is more than an order of magnitude less than the full Vbe voltage of the SET transistor.

39. (Previously Presented) The method of claim 5, wherein the second trigger signal is more than an order of magnitude less than the full Vbe voltage of the RESET transistor.